IN THE CLAIMS

1. (Currently Amended) A method for reducing false detections of access signals, comprising:

receiving a presumed access signal;

demodulating the presumed access signal;

performing equalization on an identification portion of the presumed access signal;

comparing a received sequence of bits carried by the identification portion of the presumed access signal to a reference sequence of bits;

identifying a number of received sequence of bits matching the reference sequence of bits;

determining a false detection in response to the number falling below a threshold number.

2. (Original) The method of Claim 1, further comprising:

determining an accurate detection in response to the number equaling or exceeding the threshold number.

3. (Original) The method of Claim 1, wherein the presumed access signal is a random access channel message of a Global System for Mobile Communications system.

4. (Currently Amended) A method for reducing false detections of access signals, comprising:

receiving a presumed access signal;

demodulating the presumed access signal;

performing equalization on the presumed access signal;

comparing a received sequence of bits carried by the presumed access signal to a reference sequence of bits;

identifying a number of received sequence of bits matching the reference sequence of bits;

determining a false detection in response to the number falling below a threshold number;

wherein the presumed access signal is a random access channel message of a Global System for Mobile Communications system; ~~The method of Claim 3,~~

wherein the received sequence of bits is a training sequence of the random access channel message.

5. (Original) The method of Claim 4, wherein the threshold number is 35 bits of the training sequence having 41 bits.

6. (Original) A system for reducing false detections of access signals, comprising:

a demodulator operable to receive a presumed access signal, the demodulator operable to determine a time of arrival of the presumed access signal;

an equalizer operable to perform equalization on the presumed access signal, the equalizer operable to compare a received sequence of bits carried by the presumed access signal to a reference sequence of bits, the equalizer operable to determine a number of bits of the received sequence of bits that match the reference sequence of bits, the equalizer operable to identify the presumed access signal as an actual access signal in response to the number of bits equaling or exceeding a threshold number.

7. (Original) The system of Claim 6, further comprising:

a decoder operable to decode the presumed access signal, the decoder operable to perform a cyclical redundancy code parity check on the received sequence of bits, the decoder operable to identify the presumed access signal as the actual access signal in response to a correct parity determination.

8. (Currently Amended) A system for reducing false detections of access signals, comprising:

a demodulator operable to receive a presumed access signal, the demodulator operable to determine a time of arrival of the presumed access signal;

an equalizer operable to perform equalization on the presumed access signal, the equalizer operable to compare a received sequence of bits carried by the presumed access signal to a reference sequence of bits, the equalizer operable to determine a number of bits of the received sequence of bits that match the reference sequence of bits, the equalizer operable to identify the presumed access signal as an actual access signal in response to the number of bits equaling or exceeding a threshold number;

a decoder operable to decode the presumed access signal, the decoder operable to perform a cyclical redundancy code parity check on the received sequence of bits, the decoder operable to identify the presumed access signal as the actual access signal in response to a correct parity determination; ~~The system of Claim 7,~~

wherein the decoder is operable to re-encode the presumed access signal and compare a re-encoded sequence of bits to the received sequence of bits, the decoder operable to identify the presumed access signal as the actual access signal in response to a number of received sequence of bits matching the re-encoded sequence of bits equaling or exceeding a threshold number.

9. (Currently Amended) A system for reducing false detections of access signals, comprising:

a demodulator operable to receive a presumed access signal, the demodulator operable to determine a time of arrival of the presumed access signal;

an equalizer operable to perform equalization on the presumed access signal, the equalizer operable to compare a received sequence of bits carried by the presumed access signal to a reference sequence of bits, the equalizer operable to determine a number of bits of the received sequence of bits that match the reference sequence of bits, the equalizer operable to identify the presumed access signal as an actual access signal in response to the number of bits equaling or exceeding a threshold number; ~~The system of Claim 6,~~

wherein the demodulator is operable to initially identify the presumed access signal as the actual access signal in response to identifying the time of arrival.

10. (Currently Amended) A system for reducing false detections of access signals, comprising:

a demodulator operable to receive a presumed access signal, the demodulator operable to determine a time of arrival of the presumed access signal;

an equalizer operable to perform equalization on the presumed access signal, the equalizer operable to compare a received sequence of bits carried by the presumed access signal to a reference sequence of bits, the equalizer operable to determine a number of bits of the received sequence of bits that match the reference sequence of bits, the equalizer operable to identify the presumed access signal as an actual access signal in response to the number of bits equaling or exceeding a threshold number; ~~The system of Claim 6,~~

wherein the demodulator is operable to identify the time of arrival of the presumed access signal within a first eight bits of the presumed access signal.

11. (Original) The system of Claim 6, wherein the presumed access signal is a random access channel message in a Global System for Mobile Communications system.

12. (Currently Amended) A system for reducing false detections of access signals, comprising:

a demodulator operable to receive a presumed access signal, the demodulator operable to determine a time of arrival of the presumed access signal;

an equalizer operable to perform equalization on the presumed access signal, the equalizer operable to compare a received sequence of bits carried by the presumed access signal to a reference sequence of bits, the equalizer operable to determine a number of bits of the received sequence of bits that match the reference sequence of bits, the equalizer operable to identify the presumed access signal as an actual access signal in response to the number of bits equaling or exceeding a threshold number;

wherein the presumed access signal is a random access channel message in a Global System for Mobile Communications system; ~~The system of Claim 11,~~

wherein the received sequence of bits is a training sequence of the random access channel message.

13. (Original) The system of Claim 12, wherein the training sequence is 41 bits, the 41 bits of the training sequence being compared to a reference 41 bit training sequence.

14. (Original) The system of Claim 13, wherein the threshold number is 35 of the 41 bits of the received sequence of bits matching the reference sequence of bits.

15. (Currently Amended) A system for reducing false detections of access signals, comprising:

a demodulator operable to receive a presumed access signal, the demodulator operable to determine a time of arrival of the presumed access signal;

an equalizer operable to perform equalization on the presumed access signal, the equalizer operable to compare a received sequence of bits carried by the presumed access signal to a reference sequence of bits, the equalizer operable to determine a number of bits of the received sequence of bits that match the reference sequence of bits, the equalizer operable to identify the presumed access signal as an actual access signal in response to the number of bits equaling or exceeding a threshold number; ~~The system of Claim 6,~~

wherein each bit of the received sequence of bits is compared to each bit of the reference sequence of bits, the equalizer operable to generate a positive value for each bit of the received sequence of bits matching a corresponding bit of the reference sequence of bits, the equalizer operable to sum the positive values generated in order to obtain the number for comparison with the threshold number.

16. (Original) A method of reducing false detection of access signals, comprising:

receiving a presumed access signal;

demodulating the presumed access signal;

determining a time of arrival of the presumed access signal;

discarding the presumed access signal in response to no time of arrival determination;

equalizing the presumed access signal in response to determining the time of arrival;

comparing each bit of a received sequence of bits of the presumed access signal to a corresponding bit of a reference sequence of bits;

generating a positive value for each bit of the received sequence of bits matching its corresponding bit of the reference sequence of bits;

accumulating the positive values to obtain a number;

comparing the number to a threshold number;

identifying the presumed access signal as an actual access signal in response to the number equaling or exceeding the threshold number.

17. (Original) The method of Claim 16, wherein the time of arrival is determined by establishing synchronization between a mobile unit and a base station.

18. (Original) The method of Claim 16, further comprising:

performing a cyclical redundancy code parity check on the presumed access signal;

discarding the presumed access signal in response to identifying a failure in the parity check.

19. (Original) The method of Claim 18, further comprising:

re-encoding the presumed access signal in response to identifying a successful parity check;

comparing the re-encoded presumed access signal to the received presumed access signal;

identifying a number of residual bit errors due to channel noise in response to the comparison;

discarding the presumed access signal in response to the number of bit errors exceeding a bit error threshold.

20. (Original) The method of Claim 16, further comprising:

allocating physical and logical resources associated with the actual access signal.

21. (Currently Amended) A system for reducing false detections of access signals, comprising:

means for receiving a presumed access signal;

means for demodulating the presumed access signal;

means for performing equalization on an identification portion of the presumed access signal;

means for comparing a received sequence of bits carried by the identification portion of the presumed access signal to a reference sequence of bits;

means for identifying a number of received sequence of bits matching the reference sequence of bits;

means for allocating physical and logical resources associated with the presumed access signal in response to the number equaling or exceeding a threshold number.

22. (Original) The system of Claim 21, further comprising:

means for performing a cyclical redundancy code parity check on the presumed access signal;

means for discarding the presumed access signal without resource allocation in response to identifying a failure in the parity check.

23. (Currently Amended) A system for reducing false detections of access signals, comprising:

means for receiving a presumed access signal;

means for demodulating the presumed access signal;

means for performing equalization on the presumed access signal;

means for comparing a received sequence of bits carried by the presumed access signal to a reference sequence of bits;

means for identifying a number of received sequence of bits matching the reference sequence of bits;

means for allocating physical and logical resources associated with the presumed access signal in response to the number equaling or exceeding a threshold number;

means for performing a cyclical redundancy code parity check on the presumed access signal;

means for discarding the presumed access signal without resource allocation in response to identifying a failure in the parity check; ~~The system of Claim 22, further comprising:~~

means for re-encoding the presumed access signal in response to identifying a successful parity check;

means for comparing the re-encoded presumed access signal to the received access signal;

means for identifying a number of residual bit errors between the re-encoded presumed access signal and the received presumed access signal;

means for discarding the presumed access signal in response to the number of residual bit errors exceeding a bit error threshold.

24. (Currently Amended) A system for reducing false detections of access signals, comprising:

means for receiving a presumed access signal;

means for demodulating the presumed access signal;

means for performing equalization on the presumed access signal;

means for comparing a received sequence of bits carried by the presumed access signal to a reference sequence of bits;

means for identifying a number of received sequence of bits matching the reference sequence of bits;

means for allocating physical and logical resources associated with the presumed access signal in response to the number equaling or exceeding a threshold number; ~~The system of Claim 21, further comprising:~~

means for determining a time of arrival of the presumed access signal;

means for discarding the presumed access signal in response to not determining the time of arrival.

25. (Original) The system of Claim 21, wherein the presumed access signal is a random access channel message according to a Global System for Mobile Communications protocol.

26. (Currently Amended) Logic encoded in media for reducing false detections of access signals, the logic operable to:

receive a presumed access signal;

demodulate the presumed access signal;

perform equalization on an identification portion of the presumed access signal;

compare a received sequence of bits carried by the identification portion of the presumed access signal to a reference sequence of bits;

identify a number of received sequence of bits matching the reference sequence of bits;

allocate physical and logical resources associated with the presumed access signal in response to the number equaling or exceeding a threshold number.